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(54) Abstract Title: **Method and apparatus for boundary scan testing**

(57) A method of boundary scan testing assigns unique binary signatures 406' to 442' to at least one driver and at least one hysteretic test receiver memory of a circuit under test. Test vectors 502, 504 are created from corresponding bits of the binary signatures 406' to 442'. The test vectors are shifted into the circuit under test and the sequence of states output from the hysteretic test memories are captured. The unique binary signatures are then compared with the test output from the memories to indicate an interconnect defect in the circuit. The method may be particularly applicable to boundary scan testing of AC coupled networks, where edge detectors can be used to recreate a digital signal from an AC input.

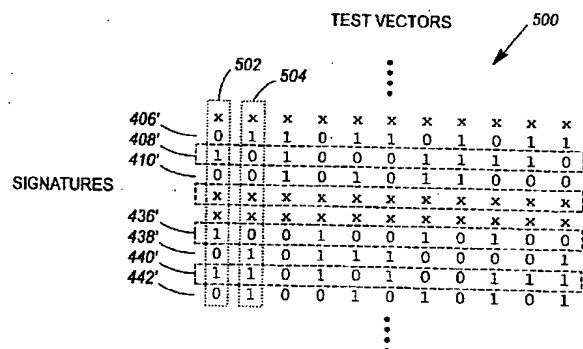


FIG. 5

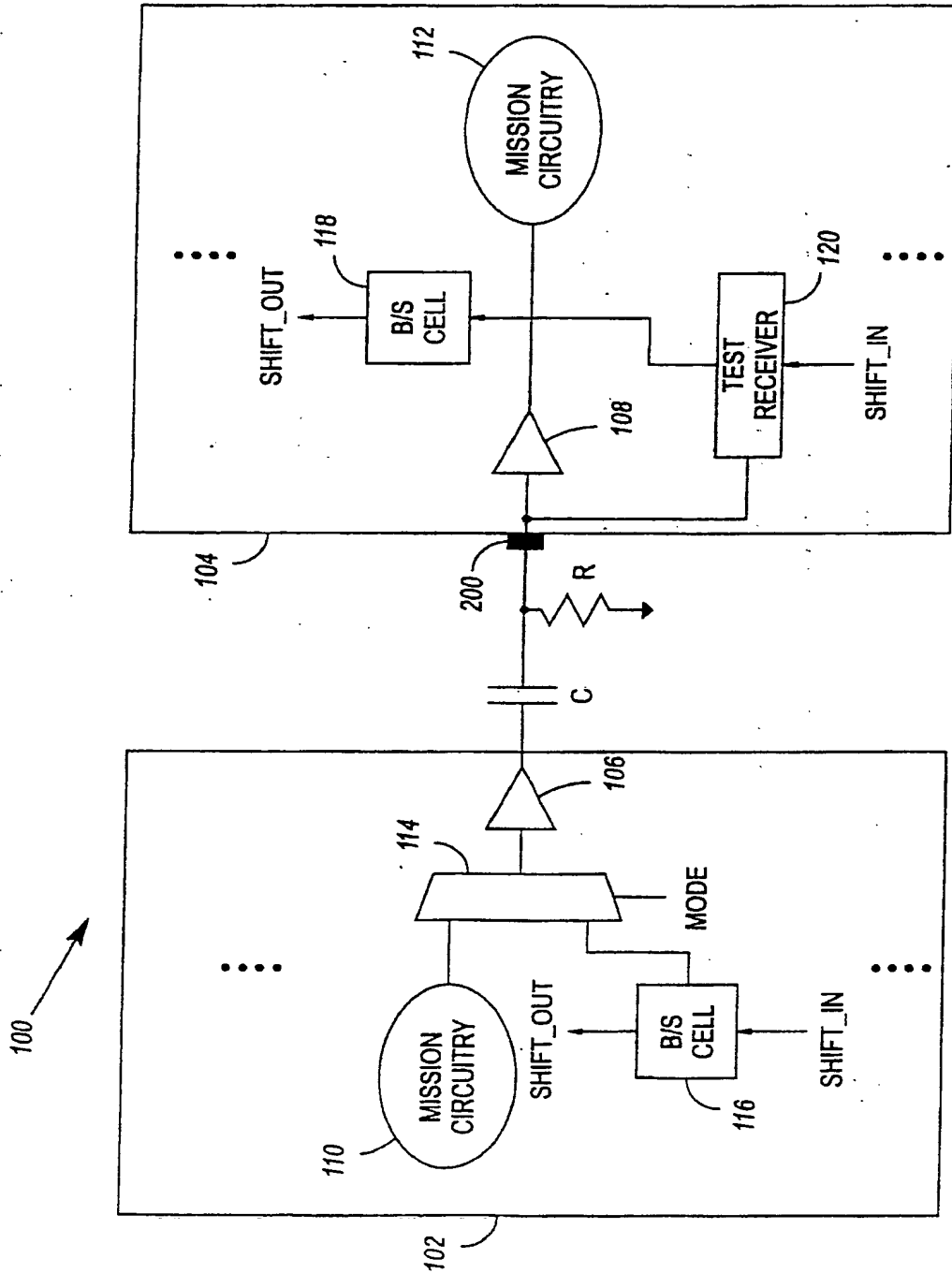


FIG. 1



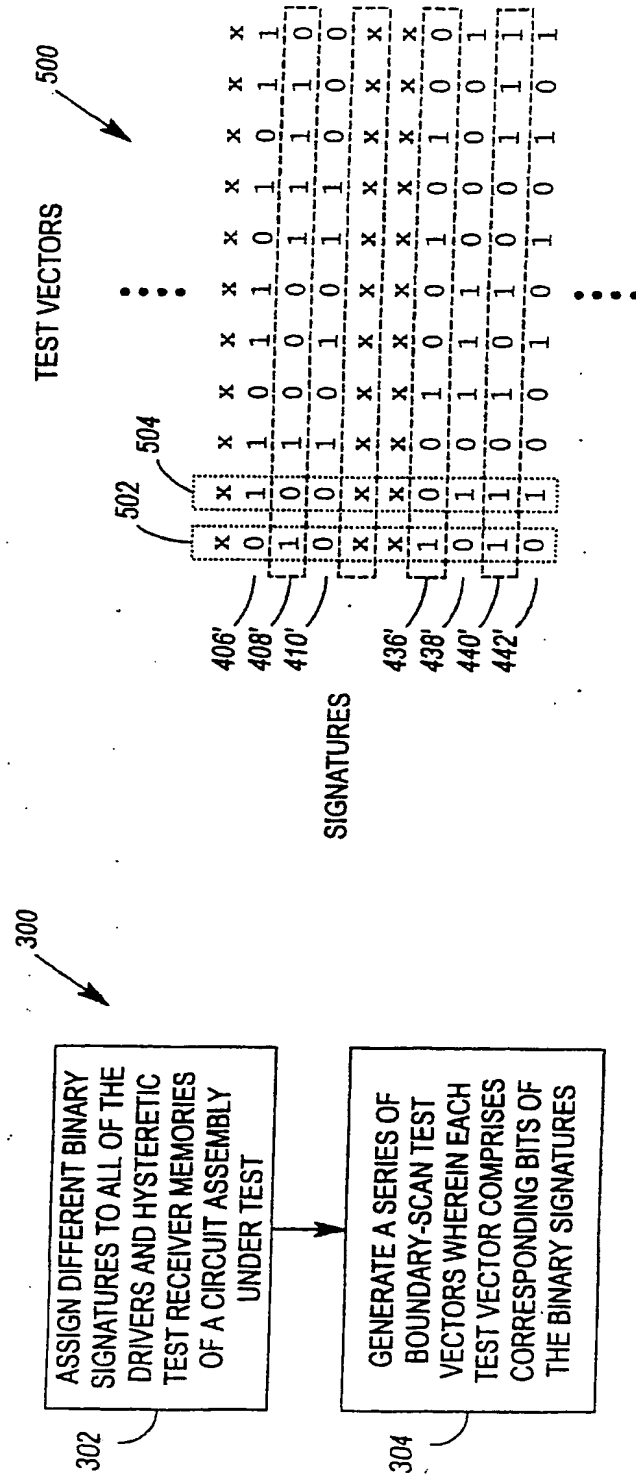
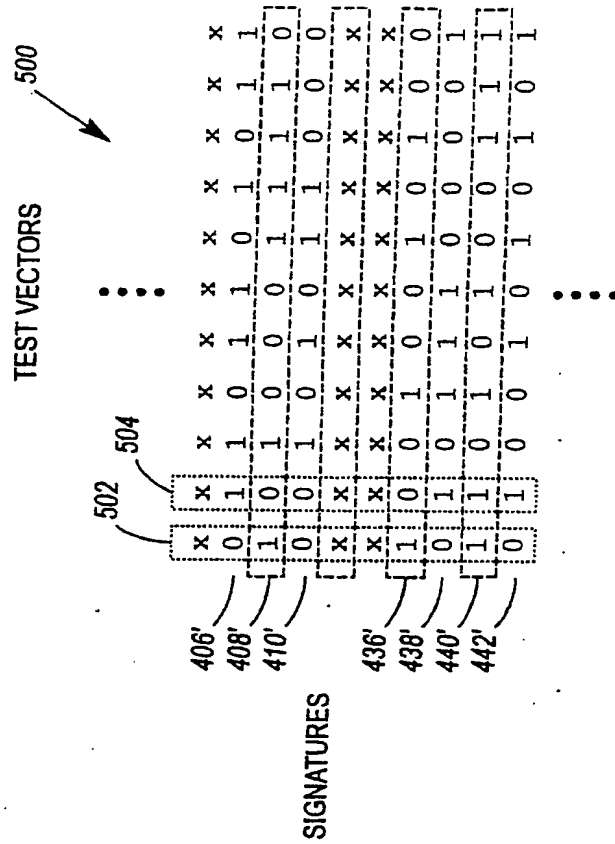


FIG. 3



**FIG. 5**

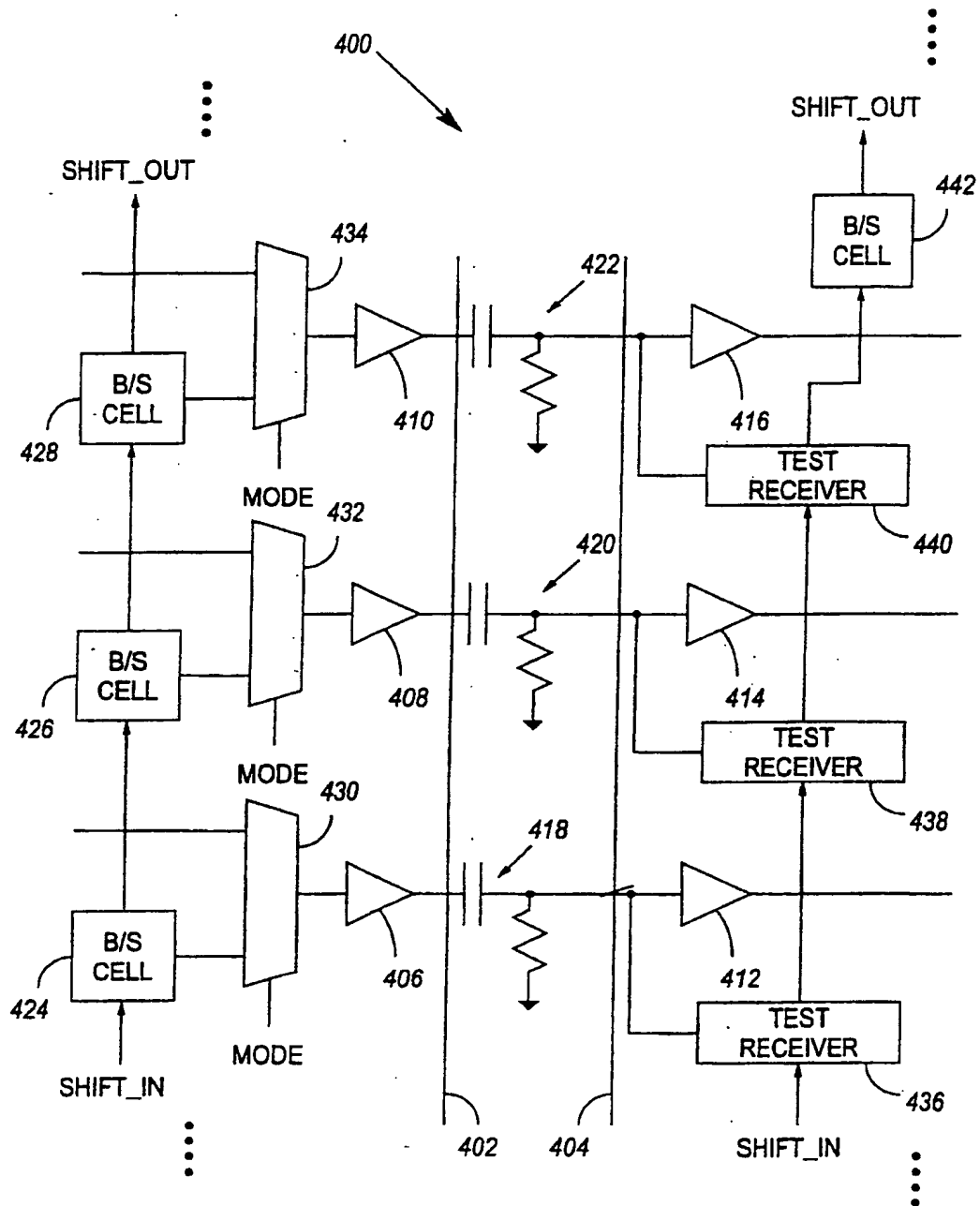


FIG. 4

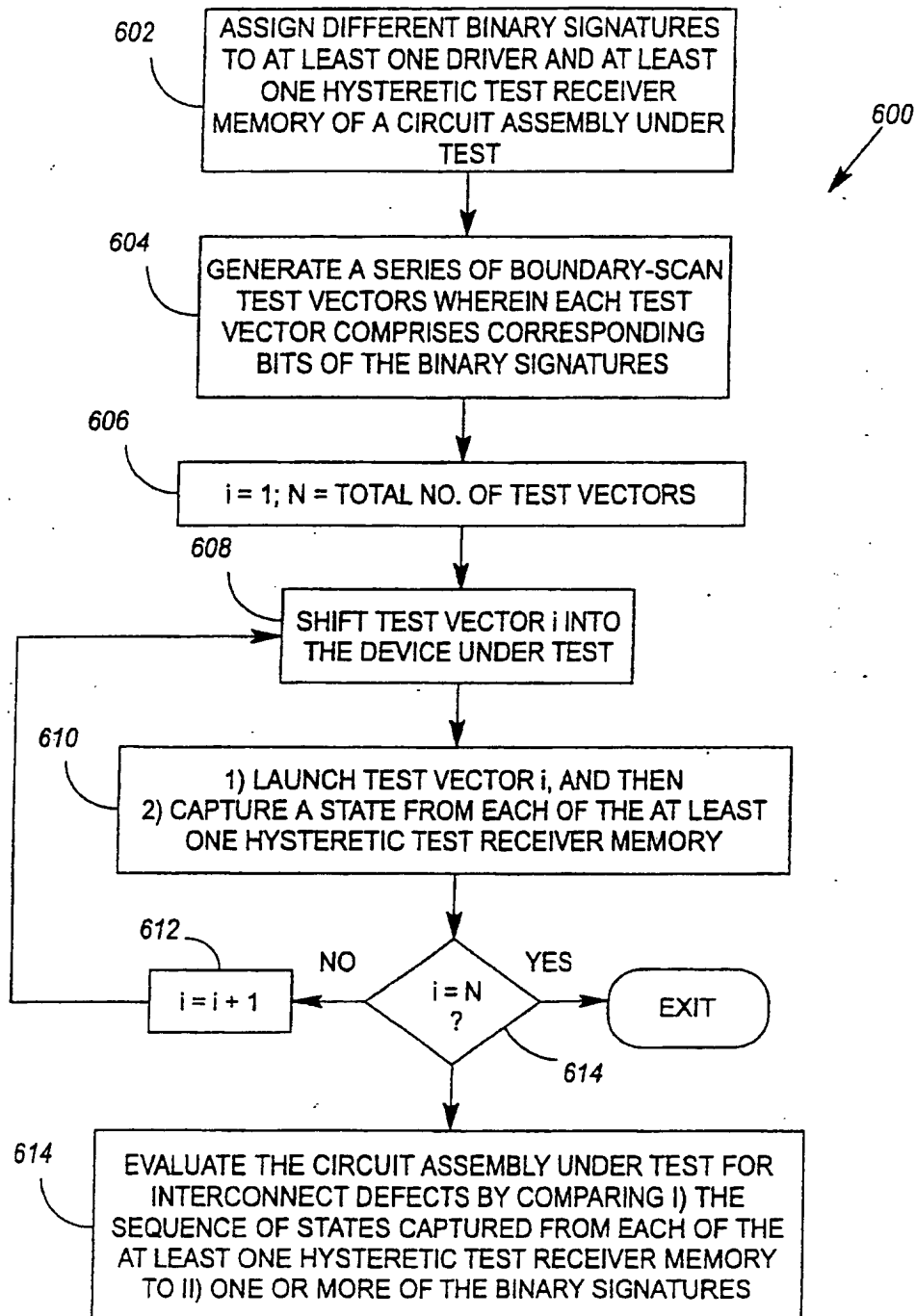


FIG. 6

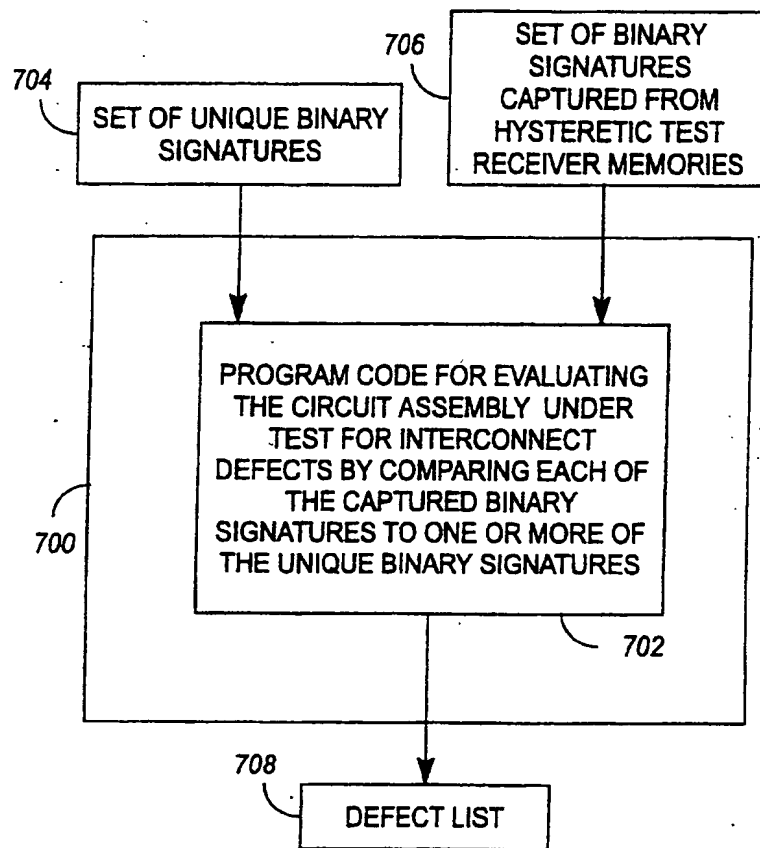


FIG. 7

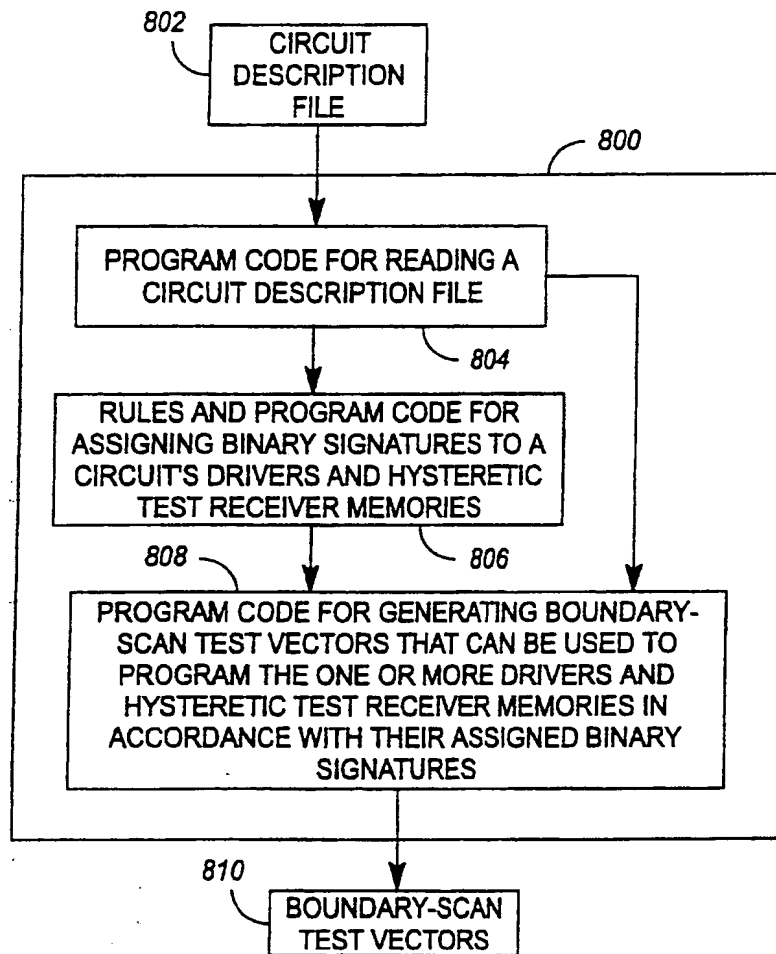


FIG. 8



## BOUNDARY-SCAN METHODS AND APPARATUS

The invention pertains to Boundary-Scan testing, and particularly, to Boundary-Scan testing of circuit assemblies comprising AC coupled networks.

10       A common way to diagnose interconnect defects (e.g., shorts and opens) in circuit assemblies (e.g., printed circuit boards, Multi-Chip Modules, and Silicon-in-Package devices) is via Boundary-Scan testing. A standard for Boundary-Scan testing is defined in IEEE Standard 1149.1.

15       As the electronics industry has moved forward with the implementation of AC coupled networks, IEEE Std. 1149.1 has become out-of-date. This is because IEEE Std. 1149.1 was drafted at a time when DC coupled networks were the norm. In an AC coupled network, for example, series capacitors are used to block DC current flow along a signal path, thereby allowing only AC signals to pass. A standard that defines how to  
20       apply Boundary-Scan techniques to AC networks is therefore needed. To this end, work is underway on IEEE Std. P1149.6 - a draft standard that addresses Boundary-Scan testing of circuit assemblies comprising AC coupled networks.

One aspect of the invention is embodied in a method for generating  
5 Boundary-Scan test vectors. The method comprises 1) assigning different  
binary signatures to all of the drivers and hysteretic test receiver memories of  
a circuit assembly under test, and 2) generating a series of Boundary-Scan  
test vectors wherein each test vector comprises corresponding bits of the  
binary signatures.

10 Another aspect of the invention is embodied in apparatus for  
evaluating a circuit assembly under test for interconnect defects. The  
apparatus comprises a number of computer readable media, and computer  
readable program code stored on the number of computer readable media.  
The computer readable program code receives 1) a set of unique binary  
15 signatures comprising data signatures assigned to drivers, and initialization  
signatures assigned to hysteretic test receiver memories, of the circuit  
assembly under test, and 2) a set of binary signatures captured from the  
hysteretic test receiver memories during Boundary-Scan testing. In  
response to these inputs, the code then evaluates the circuit assembly under  
20 test for interconnect defects by comparing each of the captured binary  
signatures to one or more of the unique binary data and initialization  
signatures.

Other embodiments of the invention are also disclosed.

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Illustrative and presently preferred embodiments of the invention are  
illustrated in the drawings in which:

30 FIG. 1 illustrates an exemplary circuit assembly comprising an AC  
coupled network;

FIG. 2 illustrates an exemplary embodiment of the test receiver shown

in FIG. 1;

FIG. 3 illustrates a first exemplary method for generating Boundary-Scan test vectors;

5       FIG. 4 illustrates an exemplary portion of a circuit assembly under test;

FIG. 5 illustrates an exemplary series of test vectors;

FIG. 6 illustrates an exemplary method for evaluating a circuit assembly under test for interconnect defects;

10       FIG. 7 illustrates an exemplary embodiment of apparatus for evaluating a circuit assembly under test for interconnect defects; and

FIG. 8 illustrates an exemplary embodiment of apparatus for generating Boundary-Scan test vectors.

15

FIG. 1 illustrates an exemplary circuit assembly 100 comprising an AC coupled network. The AC network couples a driver 106 of a first device 102 to a receiver 108 of a second device 104. By way of example, the two  
20       devices 102, 104 could be integrated circuits (ICs). The devices 102, 104 might be coupled via an AC network for a variety of reasons, such as their use of incompatible DC signal levels. In the case of incompatible DC signal levels, the receiver 108 of the second device 104 would incorporate a biasing network for the purpose of establishing its own preferred operating  
25       point, typically at the midpoint of its logic swing.

The AC coupling of the FIG. 1 circuit assembly 100 comprises a capacitor (C) that is coupled in series with the driver 106 of the first device 102 and the receiver 108 of the second device 104. The AC coupling might further comprise a termination resistor (R).

30       Although FIG. 1 only illustrates one AC coupling between the devices 102, 104 shown, in practice, the two devices 102, 104 would likely be coupled by a plurality of AC couplings, and quite possibly, a mix of AC and

DC couplings.

Because AC couplings will not pass DC voltage levels, the receiver 108 in the second device 104 will see capacitive decay in transmitted signals if the rate of change of the transmitted signals is low compared to the time constant ( $R \cdot C$ ) of the coupling. Signals must therefore be transmitted at a high enough frequency, and with frequent enough transitions, so as to mitigate signal decay. To this end, the mission circuitry 110 of a transmitting device 102 will typically encode data in such a way that frequent signal transitions are assured, thus "conditioning" the AC coupling for data transfer.

Unfortunately, the transient nature of an AC coupling makes it difficult, if not impossible, to test the coupling using the Boundary-Scan principles set forth in IEEE Std. 1149.1 (sometimes referred to herein as the "1149.1 standard"). The 1149.1 standard contemplates the transmission of DC signal levels between drivers 106 and receivers 120. Although the DC signal levels are periodically changed, there is no requirement that the signal levels be changed with any particular frequency. As a result, the time between signal level changes is typically quite long in comparison to the time constant of an AC coupling. The length of time between signal level changes is due to a combination of factors, including: the frequency of the Boundary-Scan test clock (TCK) being orders of magnitude slower than a device's mission clock frequency, and a need to frequently interrupt the test clock for the processing of test system overhead functions. Since low frequency signals transmitted through an AC coupling tend to decay, conventional Boundary-Scan testing of AC coupled networks is unreliable at best, and often not even practical.

A standard for applying Boundary-Scan techniques to AC coupled networks is in the process of being developed. The preliminary draft of the standard has been identified as IEEE Std. P1149.6. The standard contemplates the creation of an AC waveform that is propagated between a mission driver 106 and a test receiver 120. Because of the variability of test clock rates and the amount of data shifting involved, the AC waveform may still be of a low frequency. However, the waveform is constructed such that

each test bit sent via the waveform comprises at least two waveform edges – first the intended test bit is sent, followed by the complement of the test bit, followed by the intended test bit again.

As illustrated in FIG. 2, the test receiver 120 contemplated by IEEE Std. P1149.6 comprises rising and falling edge detectors 202, 204 which are used to “reconstruct” an original waveform from the edges of the waveform that pass through an AC coupling. Thus, even though the DC levels produced by a driver 106 may decay, an “original” waveform may still be reconstructed by the test receiver 120. Thus, Boundary-Scan “thinks” it is testing with levels, but in reality, an AC waveform crosses over an AC coupling, and an integrator reconstructs the original waveform from its edge information.

Referring to the FIG. 2 test receiver 120 in more detail, one notices that the receiver 120 comprises two op-amps 202, 204. The upper op-amp 202 is a leading edge detector that “sets” the flip-flop 214 marked “U”. The lower op-amp 204 is a falling edge detector that “resets” the “U” flip-flop 214. Thus, an AC waveform seen in differentiated form at pin 200 is reconstructed at the output of the “U” flip-flop 214 (i.e., so long as switch 210 is in its “AC” position). The two voltage sources ( $V_{hyst}$ ) 206, 208 provide noise immunity that prevents small signal noise from being integrated. The low-pass filter ( $R_F/C_F$ ) holds the recent, average value of the incoming waveform so that the edge detectors 202, 204 can compare this value to the instantaneous value of the incoming waveform. Thus, if a signal edge arrives at pin 200, and then slowly decays, the signal edge will set (or reset) the “U” flip-flop 214. The “U” flip-flop 214 can be thought of as a “hysteretic” memory (or hysteretic test receiver memory) in that it retains the state of the last valid signal level received by the test receiver 120 - even after the signal level has decayed and may no longer exist.

During Boundary-Scan testing, the signal levels (i.e., data values) stored in the “U” flip-flop 214 need to be captured and evaluated. If the “U” flip-flop 214 is equated with the Update flip-flop of a conventional Boundary-Scan cell, then its output may be linked to the input of a Capture flip-flop

(i.e., the "C" flip-flop 212 in FIG. 2). From there, data may be shifted out of the test receiver 120. Depending on the position of the Capture flip-flop 212 in a Boundary-Scan register, its data may be shifted through other Boundary-Scan cells (e.g., cell 118, as well as other cells connected to SHIFT\_OUT).

5       The Boundary-Scan cell 212, 214 further comprises a multiplexer 216. A first path through the multiplexer links the output of the Update flip-flop 214 to the input of the Capture flip-flop 212. A second path through the multiplexer links the input of the Capture flip-flop 212 to upstream Boundary-Scan cells forming a part of the afore-mentioned Boundary-Scan register  
10       (i.e., cells connected to SHIFT\_IN). A control signal (ShiftDR) determines which of the two paths is active. If the second path is active (ShiftDR=1), data appearing at SHIFT\_IN may be shifted into the Capture flip-flop 212 in sync with the control signal ClockDR, and then loaded into the Update flip-flop 214 (i.e., the hysteretic test receiver memory) in sync with the control  
15       signal UpdateDR.

      During Boundary-Scan testing, the hysteretic memory 214 of a test receiver 120 is preferably "preset" or "initialized" to a known state. This is a relatively easy task when the test receiver 120 incorporates a Boundary-Scan cell 212-216 – a known initial state is merely merged into a Boundary-  
20       Scan test vector, shifted into a test receiver's Boundary-Scan cell, and then loaded into the test receiver's hysteretic memory 214. The shifting and loading of a test vector may be accomplished via Boundary-Scan instructions such as PRELOAD or EXTEST.

      Although IEEE Std. P1149.6 discusses the need to initialize hysteretic  
25       test receiver memories 214, and discloses that initialization can be accomplished by means of Boundary-Scan test vectors, the draft standard provides little guidance on "choosing" a hysteretic memory's initial state(s).

      Mere "initialization" of hysteretic memories 214 is not enough to ensure adequate failure diagnosis of a circuit assembly under test. For  
30       example, if a hysteretic test receiver memory 214 is initialized to a logic low, and its initialized value does not change, there is no way to determine whether 1) the memory 214 has been "reset" to a logic low, or 2) the memory

214 has merely retained its initialization value. Likewise, if the memory 214 is initialized to a logic high, there is no way to determine whether 1) the memory 214 has been "set" to a logic high, or 2) the memory 214 has merely retained its initialization value. Thus, some way of choosing a hysteretic memory's state at each opportunity to preset the memory 214 is needed.

In recognition of the above need, FIG. 3 illustrates a first exemplary method 300 for generating Boundary-Scan test vectors. The method 300 commences with the assignment 302 of different binary signatures to all of the drivers and hysteretic test receiver memories of a circuit assembly under test. A series of Boundary-Scan test vectors is then generated 304, wherein each test vector comprises corresponding bits of the binary signatures.

FIGS. 4 & 5 illustrate how the FIG. 3 method might actually be applied to a circuit assembly under test. FIG. 4 illustrates a portion 400 of the circuit assembly under test. The circuit assembly under test comprises two devices 402, 404, one of which comprises three drivers 406-410, and one of which comprises three receivers 412-416. Each of the drivers 406-410 is coupled to a corresponding receiver 412-416 via an AC coupling 418-422.

Each driver 406-410 is coupled to a corresponding Boundary-Scan cell 424-428 via a multiplexer 430-434. The multiplexers 430-434 alternately couple the drivers 406-410 to their corresponding Boundary-Scan cells 424-428, or to mission logic, depending on the state of a MODE signal.

Coupled to the input of each receiver 412-416 is a corresponding test receiver 436-440. Each test receiver 436-440 may be configured as shown in FIG. 2 (or in other ways) and comprises hysteretic memory that is integrated with a Boundary-Scan cell.

The Boundary-Scan cells of a circuit assembly under test may be linked via any number of scan chains. By way of example, FIG. 4 illustrates a first scan chain linking the driver cells 424-428 of one device 402 and a second chain linking the test receiver cells 436-440 of another device 404. Also by way of example, FIG. 4 illustrates the second scan chain's inclusion of a "non-test receiver" Boundary-Scan cell 442 (e.g., a Boundary-Scan cell that monitors the output of a DC coupled receiver). The "non-test receiver"

Boundary-Scan cell 442 illustrates that non-uniform types of Boundary-Scan cells 436-442 may be linked together in the same scan chain.

FIG. 5 illustrates the various binary signatures 406'-442' that may be assigned to the drivers and hysteretic test receiver memories of the circuit assembly under test in FIG. 4. The signatures 406'-442' read from left-to-right and are identified by the prime of their corresponding driver's or test receiver's reference number. Thus, the binary signature 406' assigned to driver 406 is "01101101011". As indicated by FIG. 5's ellipses, only a portion of the signatures assigned to a circuit assembly under test are shown. The "x"s in FIG. 5 are not intended to be "don't cares", but rather reflect signatures corresponding to Boundary-Scan cells that are not shown in FIG. 5.

After each driver and hysteretic test receiver memory has been assigned a signature, a series of Boundary-Scan test vectors 502, 504 may be generated by grouping corresponding bits of the signatures.

Having generated a series of Boundary-Scan test vectors 502, 504, the vectors may then be used to evaluate a circuit assembly under test for interconnect defects. FIG. 6 illustrates such a method 600. The method 600 begins similarly to the method illustrated in FIG. 3. That is, different binary signatures are assigned 602 to at least one driver and at least one hysteretic test receiver memory of the circuit assembly under test, and then a series of Boundary-Scan test vectors is generated 604 (wherein each test vector comprises corresponding bits of the binary signatures). Thereafter, the test vectors are shifted 606, 608, 612, 614 into a circuit assembly under test. For the purpose of this disclosure, bits of a test vector are considered shifted into a driver (e.g., driver 406, FIG. 4) when they are shifted into the driver's corresponding Boundary-Scan cell (e.g., cell 424).

After shifting each test vector into the circuit assembly under test, the test vector is launched 610, and a state is captured 610 from each of the circuit assembly's hysteretic test receiver memories 436-442. The circuit assembly under test may then be evaluated 614 for interconnect defects by comparing 1) the sequence of states captured from each hysteretic test



receiver memory to 2) one or more of the binary signatures.

Apparatus for evaluating a circuit assembly under test for interconnect defects is shown in FIG. 7. The apparatus is embodied in computer readable program code 702 stored on a number of computer readable media  
5 700. The computer readable program code 702 receives 1) a set of unique binary signatures 704 comprising data signatures assigned to drivers, and initialization signatures assigned to hysteretic test receiver memories, of the circuit assembly under test, and 2) a set of binary signatures 706 captured from the hysteretic test receiver memories during Boundary-Scan testing.  
10 The unique binary signatures 704 may be generated in accordance with the methods of FIG. 3 or FIG. 5, for example. The captured binary signatures 706 are equivalent to the sequences of captured states disclosed in FIG. 5.

The FIG. 7 apparatus evaluates the circuit assembly under test for interconnect defects by comparing the captured binary signatures it receives  
15 to one or more of the unique binary data and initialization signatures it receives. Since each driver and hysteretic test receiver memory is assigned a unique binary signature, the binary signature captured from a hysteretic test receiver memory should match the unique binary data signature of its corresponding driver. If the two signatures do not match, the FIG. 7  
20 apparatus notes an interconnect defect.

If an interconnect defect is noted, additional steps may be taken to determine the type of interconnect defect. For example, the binary signature captured from a hysteretic test receiver memory may be compared to the unique binary data signatures for one or more drivers, and a short may be  
25 noted if any two signatures match. The binary signature captured from a hysteretic test receiver memory may also be compared to the unique binary initialization signatures for one or more other hysteretic receiver memories, with a short again being noted if any two signatures match. The binary signature captured from a hysteretic test receiver memory may be further  
30 compared to its own unique binary initialization signature, with an open being noted if the two signatures match.

To ensure that the state of a hysteretic test receiver memory is

frequently "wiggled", the binary signature assigned to a hysteretic test receiver memory may be selected such that it is the complement of a sequence of states that is expected to be captured from the hysteretic test receiver memory as a series of test vectors is launched in a circuit assembly under test. Put another way, and assuming that a hysteretic test receiver memory is non-inverting, the signature assigned to the hysteretic test receiver memory may be selected such that it is the complement of the signature assigned to its corresponding driver. In this manner, the evaluation apparatus illustrated in FIG. 7 may determine if the binary signature captured from a hysteretic test receiver memory is the complement of the memory's initialization signature, and note an interconnect defect if not.

In accordance with the method for generating Boundary-Scan test vectors illustrated in FIG. 3, FIG. 8 illustrates apparatus for generating Boundary-Scan test vectors. The apparatus is embodied in computer readable program code 804, 806, 808 stored on a number of computer readable media 800. The computer readable program code 804 comprises code for reading a circuit description file 802, rules and code 806 for assigning binary signatures to a circuit's drivers and hysteretic test receiver memories, and code 808 for generating Boundary-Scan test vectors 810. The circuit description file 802 describes a circuit comprising one or more drivers and one or more hysteretic test receiver memories. The rules 806 may be more or less complex, but at least require the assignment of different binary signatures to a corresponding driver and hysteretic test receiver memory. The code 808 for generating Boundary-Scan test vectors 810 generates vectors that can be used to program the one or more drivers and one or more hysteretic test receiver memories of a circuit in accordance with their assigned binary signatures.

In alternative embodiments of the FIG. 8 apparatus, the rules 806 maintained as part of the program code are more complex. For example, the rules 806 may specify that each hysteretic test receiver memory described in the circuit description file be assigned a binary signature that is the complement of a sequence of states that is expected to be captured from the

first hysteretic test receiver memory during the capture phase of subsequent Boundary-Scan testing. Alternately (or additionally), the rules 806 may specify that each hysteretic test receiver memory described in the circuit description file be assigned a binary signature that differs from the binary  
5 signatures assigned to all other drivers and hysteretic test receiver memories described in the circuit description file.

While illustrative and presently preferred embodiments of the invention have been described in detail herein, it is to be understood that the inventive concepts may be otherwise variously embodied and employed, and  
10 that the appended claims are intended to be construed to include such variations, except as limited by the prior art.

The disclosures in United States patent application no. 10/292,267, from which this application claims priority, and in the abstract accompanying this application are incorporated herein by reference.

CLAIMS

1. A method of generating Boundary-Scan test vectors, including the steps of:
  - a) assigning different binary signatures to the drivers and hysteretic test receiver memories of a circuit assembly under test; and
  - b) generating a series of Boundary-Scan test vectors wherein each test vector comprises corresponding bits of the binary signatures.
2. A method as in claim 1, wherein the binary signature assigned to a first hysteretic test receiver memory is the complement of a sequence of states that is expected to be captured from the first hysteretic test receiver memory as the series of test vectors is launched.
3. A method of evaluating a circuit assembly under test for interconnect defects, including the steps of:
  - a) assigning different binary signatures to at least one driver and at least one hysteretic test receiver memory of the circuit assembly under test;
  - b) generating a series of Boundary-Scan test vectors wherein each test vector comprises corresponding bits of the binary signatures;
  - c) shifting the test vectors into the circuit assembly under test;
  - d) after shifting each test vector into the circuit assembly under test,
    - i) launching the test vector; and
    - ii) capturing a state from each of the at least one hysteretic test receiver memory; and
  - e) evaluating the circuit assembly under test for interconnect defects by comparing i) the sequence of states captured from each of the at least one hysteretic test receiver memory to ii) one or more of the binary signatures.
4. A method as in claim 3, wherein the binary signature assigned to a first hysteretic test receiver memory is the complement of a sequence of states that is expected

to be captured from the first hysteretic test receiver memory as the series of test vectors is launched.

5. A method as in claim 3 or 4, wherein different binary signatures are assigned to all of the drivers and hysteretic test receiver memories of the circuit assembly under test.
6. Apparatus for generating Boundary-Scan test vectors, including:
  - a) a number of computer readable media; and
  - b) computer readable program code stored on the number of computer readable media, the computer readable program code including:
    - i) code for reading a circuit description file that describes a circuit comprising one or more drivers and one or more hysteretic test receiver memories;
    - ii) rules and code for assigning binary signatures to a circuit's drivers and hysteretic test receiver memories; the rules at least requiring the assigning of different binary signatures to a corresponding driver and hysteretic test receiver memory; and
    - iii) code for generating Boundary-Scan test vectors that can be used to program the one or more drivers and one or more hysteretic test receiver memories in accordance with their assigned binary signatures.
7. Apparatus as in claim 6, wherein the rules for assigning binary signatures specify that each hysteretic test receiver memory described in the circuit description file be assigned a binary signature that is the complement of a sequence of states that is expected to be captured from the first hysteretic test receiver memory during the capture phase of subsequent Boundary-Scan testing.
8. Apparatus as in claim 6, wherein the rules for assigning binary signatures specify that each hysteretic test receiver memory described in the circuit description file

be assigned a binary signature that differs from the binary signatures assigned to all other drivers and hysteretic test receiver memories described in the circuit description file.

9. Apparatus for evaluating a circuit assembly under test for interconnect defects, includes:
  - a) a number of computer readable media; and
  - b) computer readable program code stored on the number of computer readable media, the computer readable program code receiving i) a set of unique binary signatures comprising data signatures assigned to drivers, and initialization signatures assigned to hysteretic test receiver memories, of the circuit assembly under test, and ii) a set of binary signatures captured from the hysteretic test receiver memories during Boundary-Scan testing; said code evaluating the circuit assembly under test for interconnect defects by comparing each of the captured binary signatures to one or more of the unique binary data and initialization signatures.
10. Apparatus as in claim 9, wherein the computer readable program code is operable to compare the binary signature captured from a hysteretic test receiver memory to the unique binary data signature for a corresponding driver, and notes an interconnected defect if the two signatures do not match.
11. Apparatus as in claim 9, wherein the computer readable program code is operable to compare the binary signature captured from a hysteretic test receiver memory to the unique binary data signatures for one or more drivers, and notes a short if any two signatures match.
12. Apparatus as in claim 9, wherein the computer readable program code is operable to compare the binary signature captured from a hysteretic test receiver

memory to the unique binary initialization signatures for one or more other hysteretic test receiver memories, and notes a short if any two signatures match.

13. Apparatus as in claim 9, wherein the computer readable program code is operable to compare the binary signature captured from a hysteretic test receiver memory to the unique binary initialization signature for the hysteretic test receiver memory, and notes an open if the two signatures match.
14. Apparatus as in claim 9, wherein the computer readable program code is operable to determine if the binary signature captured from a hysteretic test receiver memory is the complement of the unique binary initialization signature for the hysteretic test receiver memory, and notes an interconnect defect if not.
15. A method of generating Boundary-Scan test vectors substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.
16. Apparatus for generating Boundary-Scan test vectors substantially as hereinbefore described with reference to and as illustrated in the accompanying drawings.



INVESTOR IN PEOPLE

Application No: GB 0323835.9  
Claims searched: 1 to 8, 15, 16

16

Examiner: Ian Rees  
Date of search: 17 February 2004

## Patents Act 1977 : Search Report under Section 17

### Documents considered to be relevant:

Category	Relevant to claims	Identity of document and passage or figure of particular relevance
A		US 4183460 YUEN. See column 1 (lines 38 to 59).
A		US 4853928 WILLIAMS. See figure 1.

### Categories:

X Document indicating lack of novelty or inventive step	A Document indicating technological background and/or state of the art.
Y Document indicating lack of inventive step if combined with one or more other documents of same category.	P Document published on or after the declared priority date but before the filing date of this invention.
& Member of the same patent family	E Patent document published on or after, but with priority date earlier than, the filing date of this application.

### Field of Search:

Search of GB, EP, WO & US patent documents classified in the following areas of the UKC<sup>W</sup>:

G1U

Worldwide search of patent documents classified in the following areas of the IPC<sup>7</sup>:

G01R

The following online and other databases have been used in the preparation of this search report:

WPI, EPODOC, PAJ



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